REMARKS

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1, 7, 12 and 14 have been amended. Claims 1-18 are pending in this application.

Claim 14 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In response, Applicant has amended claim 14 to more clearly define the invention. Applicant submits that claim 14 is now in full compliance with 35 U.S.C. §112, second paragraph. Withdrawal of the rejection is respectfully requested.

Claims 1-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Horii in view of Applicant's prior art. Applicant traverses the rejection in view of the amendments to the claims.

Independent claims 1, 7 and 12 have been amended and now recite that the lower electrode is formed by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device. The reason for using the DC pulse instead of a continuous current such as a sine wave type current is that a dense Pt stack can be obtained and a uniform film can be obtained because of the uniform current distribution. As a result, a lower electrode of a good

quality can be obtained and thereby, a leakage current can be more effectively prevented.

Applicant submits that neither Horii nor Applicant's prior art describe this limitation. Accordingly, independent claims 1, 7 and 12, and their dependent claims 2-6, 8-11 and 13-18 are not made obvious over Horii in view of Applicant's prior art under 35 U.S.C. §103(a).

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "Version with Markings to Show Changes Made."

All objections and rejections having been addressed, it is respectfully submitted that claims 1-18 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

By: _____

Yoon S. Ham
Reg. No. 45,307
Direct Tel.: (202) 662-8483

JACOBSON HOLMAN PLLC
The Jenifer Building
400 Seventh Street, N.W.
Washington, D.C. 20004-2201
(202) 638-6666
Atty. Docket: P66792US0
YSH:dj

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 7, 12 and 14 as follows:

1. (Twice Amended) A semiconductor memory device, comprising:

a semiconductor substrate, a gate electrode formed on the semiconductor substrate, and a plurality of source/drain junctions formed in the semiconductor substrate;

an interlayer insulating layer formed over the semiconductor substrate;

a plug formed in the interlayer insulating layer, the plug [includes] including a diffusion barrier layer and a seed layer for electro plating;

a lower electrode of a capacitor contacted to the seed layer, wherein the lower electrode is formed by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

7. (Twice Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer and forming contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a lower electrode of a capacitor contacted to the seed layer by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

12. (Twice Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer and forming a contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a glue layer on the seed layer and the interlayer insulating layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer and forming an opening defining a region of a lower electrode of a capacitor;

forming the lower electrode on the seed layer in the opening, by using an electro plating technique <u>while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device</u>;

removing the sacrificial layer and the glue layer;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

14. (Amended) The method as recited in claim 13, the step of providing the semiconductor substrate including:

forming a conducting layer on the semiconductor substrate, wherein the conducting layer [plays] <u>is used as</u> an electrode in the step of forming the lower electrode.